IDLE LED -- Poetry in Motion

A Poem in 64 Words

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     ; ----- VECTORS -----
000  NOP
002  BR 170
004  000014
006  000357
010  000174
012  000341
     ; ===== TRAP4 =====
■ 014 SCC
  016 MOVB @#6,2(SP)
  024 RTI
  026 000340
     ; ----- SETUP -----
● 030 MOV #400,R5
  034 MOV #177570,R4
  040 MOV (R4),R3
  042 MOV #130,R0
  046 MOV (R0),(R5)
  050 MOV (PC)+,-(R5)
■ 052 WAIT
▲ 054 TSTB R3
● 056 BPL 104
     ; ----- FILMEM -----
  060 MOV R5,SP
▲ 062 MOV (R5),R2
▲ 064 MOV R2,(SP)+
▲ 066 BIC (SP),(SP)
▲ 070 BPL 64
▲ 072 MOV (R0)+,-14(SP)
     ; ===== VEC100 =====
■ 076 BITB #132,@#340
  100 000132
  102 000340
     ; ----- SETPAT -----
● 104 MOV #170017,-(SP)
  110 MOV SP,R1
● 112 CLR -(SP)
     ; ===== ENACLK =====
▲ 114 MOV #100,@#177546
  122 CLR R2
▲ 124 MOV #140246,-(R2)
  130 JMP (R5)
     ; ----- CLKINT -----
● 132 CMPB (R4),R3
  134 BNE 174
  136 DECB R2
■ 140 BPL 166
▲ 142 MOV (R1),R0
● 144 ASLB (R1)+
● 146 RORB (R1)
● 150 ADCB -(R1)
● 152 DEC -(R1)
▲ 154 MOV (R1)+,(R4)
  156 MOV R3,R2
  160 COMB R2
▲ 162 BICB #133300,R2
  166 RTI
     ; ===== INITSP =====
  170 MOV (PC),SP
  172 000704
  172 BR 4
  174 MOV (PC),SP
  176 000714
● 176 BR 30
```

IDLED

	Switch Register	
▲	SR7 ON	Multi-mode [overwrite memory]
▲	SR7 OFF	Single-mode [preserve memory]
▲	SR6 ON	Enable IDLED+
▲	SR6 OFF	Disable IDLED+ (keep patterns)
	SR5-SR0	Pattern rotation speed

PDP-11/70 DATA Knob	
DATA PATHS	- Show idle pattern
DISPLAY REGISTER	- Show counter

	Vectors			
	Address	PC	PSW	Description
	000004	000014	000357	Time-out etc.
	000010	000174	000341	Illegal instr.
	000024	000002	000340	Power fail
	000100	000132	000340	Line-time clock
▲	000114	012737	000100	Memory parity

	Stacks		
	Address	SP	Range
	000172	000704	000700[1]-000703
	000176	000714	000702[1]-000713
▲	MMSP[2]	xx7774	xx7766[1]-xx7773

Registers	
R0 =	Pattern for WAIT
R1 =	^Pattern double-word
R2 =	Clock tick count-down (low-byte)
R3 =	Last switch settings
R4 =	^Switch Register (177570)
R5 =	^WAIT loop start (SINGAD-2)

Stack while in CLKINT	
-2(SP)	Reserved for pattern call-out
0(SP)	Interrupted PC
2(SP)	Interrupted PSW
4(SP)	Pattern double-word …
6(SP)	… also pointed to by R1

Pattern Double-word	
-2(R1)	Current display register pat.
(R1)	Next idle [DATA LEDs] pattern

● Standard Patch		
Address	Name	Type
000032	SINGAD	(D)
000056	MMODE	(I)
000106	SETWT	(D)
000112	SETDR	(I)
000132	HIGHSR	(I)
000144	ROTATE	(I)
000146	"	(I)
000150	"	(I)
000152	UPDDR	(I)
000176	PLUSEN	(I,D)

▲ Special Patch		
Address	Name	Type
000054	MMSR	(I)
000062	FILMEM	(I)
000064	"	(I)
000066	"	(I)
000070	"	(I)
000074	MMBACK	(D)
000116	FIXODD	(P)
000126	NEWPSW	(P)
000142	PREPWT	(I)
000154	SHOWDR	(I)
000164	SPEEDM	(D)

■ Debug Patch		
Address	Name	Type
000014	HALT4	(I)
000052	WAITSM	(I,D)
000076	SKIP	(I)
000140	HLTCLK	(I)

(D) = Data (word)
(I) = Instruction
(P) = PSW

Your Thoughts

Notes for Stacks

[1] An extra 4 bytes could be overwritten by a further int.

[2] xx is 01 for 4KW up to 15 for 28KW